ANS2

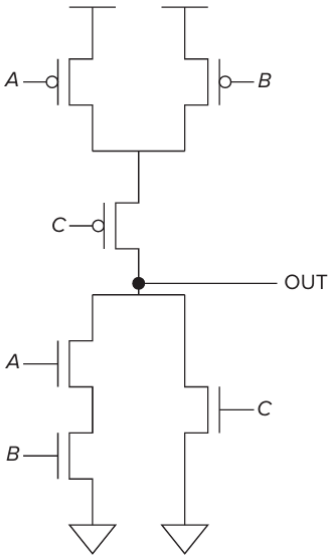
T1

$$NOT(A) = \overline{A} = \overline{A + A}$$

$$AND(A, B) = A \cdot B = \overline{\overline{A} + \overline{B}} = NOR(NOT(A), NOT(B))$$

$$OR(A, B) = A + B = \overline{\overline{A + B}} = NOT(NOR(A, B))$$

T2



A	B	C		OUT
0	0	0		1
0	0	1		0
0	1	0		1
0	1	1		0
1	0	0		1
1	0	1		0
1	1	0		0
1	1	1		0

T3

- 0 OR X = X
- 1 OR X = 1
- 0 AND X = 0
- 1 AND X = X
- 0 XOR X = X

T4

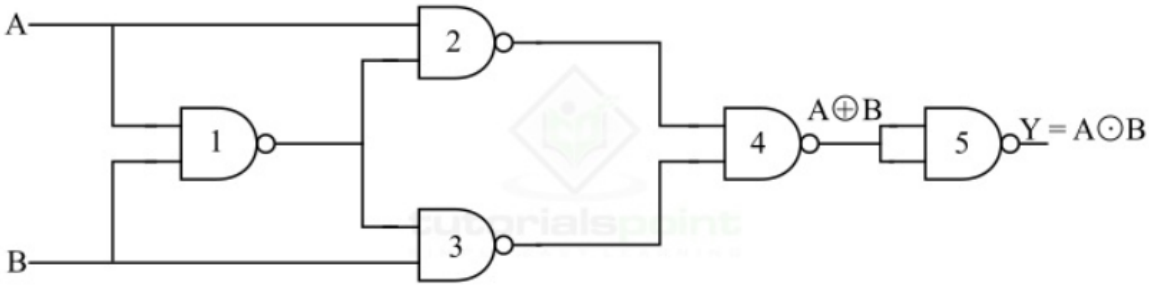


Figure 3 - XNOR Gate using NAND Gates

From the logic circuit diagram of the XNOR gate using NAND gates only, it is clear that we require 5 NAND gates.

Now, let us understand how this NAND logic circuit functions to produce an output equivalent to the XNOR gate –

The output of the first NAND gate is,

$$Y_1 = \overline{A\,B}$$

The outputs of the secondary and third NAND gates are,

$$Y_2 = \overline{A \cdot \overline{AB}}$$

$$Y_3 = \overline{B \cdot \overline{AB}}$$

These two outputs (Y2 and Y3) are connected to the fourth NAND gate. This NAND gate will produce an output which is,

$$Y = \overline{\overline{A \cdot \overline{AB}} \cdot \overline{B \cdot \overline{AB}}}$$

$$\Rightarrow Y = A \cdot \overline{AB} + B \cdot \overline{AB} = A(\bar{A} + \bar{B}) + B(\bar{A} + \bar{B})$$

$$\Rightarrow Y = A\,\bar{A} + A\,\bar{B} + \bar{A}\,B + B\,\bar{B}$$

$$\therefore Y = A\,\bar{B} + \bar{A}\,B = A \oplus B$$

Finally, the output of the fourth NAND gate is input to the fifth NAND gate that functions as an inverter, and produces an output equivalent to the XNOR gate, i.e.,

$$Y = \overline{A \oplus B} = A \odot B$$

T5

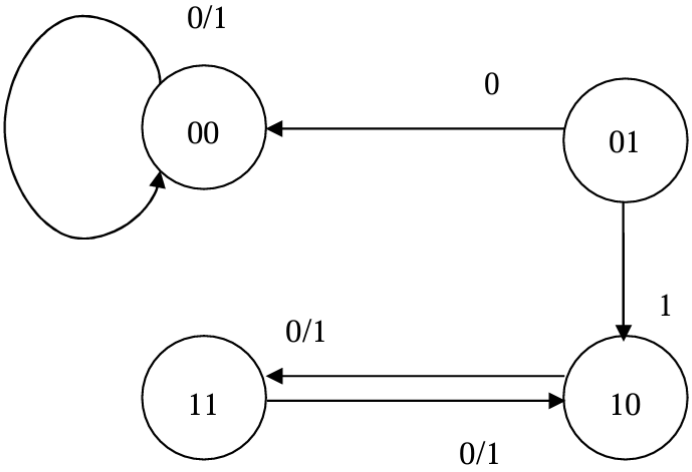
1.
   - 3
   - 4
   - 0111
2. 8 * (2^4) = 128 bytes

T6

1.

S1	S0	X		D1	D0	Z
0	0	0		0	0	0
0	0	1		0	0	0
0	1	0		0	0	1
0	1	1		1	0	1
1	0	0		1	1	1
1	0	1		1	1	1
1	1	0		1	0	1
1	1	1		1	0	1

2.



T7

opcode 有 56 条，则需要 6bit 才能表示完整。 register 有 40 个，也需要 6bit 才能表示完整。 则 IMM 可用位数为： 32 - 6 - 6 - 6 = 14bit，表示范围:

$$-2^{13} < IMM < 2^{13} - 1$$

T8

		F	D	EA	FO	E	SR	
x86	ADD [eax] edx	50	1	1	50	1	50	153
LC3	ADD R6, R2, R6	50	1	-	1	1	1	54

T9

1. MAR: x2 MDR: 01010000
2. MDR: 00111001